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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/780,634	02/09/2001	Erik R. Altman	YOR9-2000-0845 US1 (8728-	9328

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EXAMINER	
WANG, ALBERT C	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 06/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/780,634	ALTMAN ET AL.	
	Examiner	Art Unit	
	Albert Wang	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication..
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-18 and 20-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-18 and 20-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *21 November 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is responsive to Amendment A filed March 26, 2004. Applicant has amended independent claims 1, 9 and 17, canceled claims 3 and 19, and added new claims 21 and 22. Claims 1, 2, 4-18 and 20-22 are pending.

2. Applicant's arguments with respect to claims 1, 2, 4-18 and 20-22 have been considered but are moot in view of the new ground(s) of rejection.

3. In the remarks with respect to claims 17, 18 and 20, Applicant argues in substance that Bartley does not teach "the value of the comparing step includes a number determined to provide net power savings in the logical circuits". The rejection of claim 17 has been rewritten by citing a new passage (Col. 7, lines 11-21) to clarify that Bartley's predetermined threshold is determined to provide such net power savings.

Claim Objections

4. Claims 1, 6, 7 and 21 are objected to because of the following informalities: "logical circuit", "logical unit" and "logical device" are interpreted as "logic circuit". Appropriate correction is required.

5. Claim 9 is objected to because of the following informalities: "logic groups" in the last line is interpreted as "functional groups". Appropriate correction is required.

6. Claims 17 and 18 are objected to because of the following informalities: "logical circuits" is interpreted as "logic circuits". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 4, 7, 9, 11, 12, 15 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Gupta et al., U.S. Patent No. 5,996,083 ("Gupta"), which is prior art cited by the Applicant in the IDS filed November 21, 2003.

As per claim 1, Gupta discloses a microprocessor (Fig. 2, microprocessor 100), comprising:

at least one logic circuit (Figs. 2 & 6, functional units FU_1- FU_N);

a selection device coupled to the at least one logic circuit, the selection device providing switching of on/off states of the at least one logic circuit based on a stored logical value, wherein the selection device includes a switch which provides a connection from ground to a power line of the at least one logic circuit in an on state (Fig. 6, selection device includes transistor 158 which provides switching and provides connection to ground based on value stored in power control register field 108; Col. 7, line 55 – Col. 8, line 14); and

a program instruction which sets the stored logical value to control the on/off states of the at least one logic circuit based on anticipated usage of the at least one logical circuit in accordance with an instruction sequence of the microprocessor (Col. 5, lines 39-57, usage of functional units is based on instruction code of microprocessor; Col. 11, line 58 – Col. 12, line 1, software adjusts value for power control register field according to future usage of functional units).

As per claim 4, Gupta discloses a register coupled to the selection device to store the logical value (Fig. 6, power control register).

As per claim 7, Gupta discloses the anticipated usage of the at least one logical unit includes usage after a number of instruction cycles (Col. 11, line 58 – Col. 12, line 1, looking further cycles into the future).

As per claim 22, Gupta discloses a register is coupled to a plurality of logic circuits, including the at least one logic circuit through corresponding selection devices (Fig. 2, power control register 106; Col. 7, line 55 – Col. 8, line 14).

As per claim 9, Gupta discloses a microprocessor (Fig. 2, microprocessor 100), comprising:

a plurality of logic circuits divided into functional groups (Figs. 2 & 6, functional units FU_1- FU_N);

a selection device coupled to each of the functional groups, each selection device providing switching of on/off states of the corresponding functional group based on logical values stored in a register, wherein the register is coupled to each functional unit group through a corresponding selection device (Fig. 6, transistor 158 provides switching of functional unit FU1 based on value stored in field 108 of power control register);

a program instruction which sets the logical values in the register to control the on/off states of the functional groups (Col. 5, lines 60-65, software sets logical values in the register); and

a compiler program which generates the logical values to be set in the register based on instruction sequences which anticipate usage of each of the functional groups

(Col. 11, line 58 – Col. 12, line 1, software adjusts value for power control register field according to future usage of functional units).

As per claim 11, Gupta discloses the selection devices each include a switch that provides a connection from ground to a power line of the functional group in an on state (Fig. 6, transistors provide connection to ground)

As per claim 12, Gupta discloses the register includes one memory location for each function group (Fig. 2; Col. 6, lines 1-14).

As per claim 15, Gupta discloses the usage of the functional groups includes usage of the functional groups after a number of instruction cycles (Col. 11, line 58 – Col. 12, line 1, looking further cycles into the future).

8. Claims 17, 18, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Bartley, U.S. Patent No. 6,219,796. Bartley was cited in the previous office action.

As per claim 17, Bartley discloses a method for generating embedded instruction sequences to control power to logic circuits in a microprocessor, comprising the steps of:

generating an instruction sequence which controls a functional program for the microprocessor (Fig. 7, code sequence is generated prior to scan step; Col. 4, lines 15-19);

analyzing the instruction sequence to determine which of the logic circuits are active on each instruction cycle (Fig. 7, inactive segments are determined for each functional unit);

comparing a number of instruction cycles for which each logic circuit will be inactive after a current instruction cycle to a value for each instruction cycle of the

functional program (Col. 7, lines 39-46, duration of inactive segments is compared to predetermined threshold), wherein the value of the comparing step includes a number determined to provide net power savings in the logical circuits (Col. 7, lines 11-21, predetermined threshold is length of time during which it is more efficient to turn logic circuit off); and

inserting instruction sequences to turn each of the logical circuits on or off based on the comparing step (Fig. 7, insert power-down/up instruction to functional unit).

As per claim 18, Bartley discloses the step of inserting instruction sequences includes programming a register with logical values wherein each of the logical circuits are turned on or off based on the logical values (Fig. 2; Col. 5, lines 55-65).

As per claim 20, Bartley discloses a program storage device readable by machine, tangibly embodying a program of instructions executable by the machine (Fig. 1, program memory 12).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2, 5, 10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta as applied to claims 1 and 9 above, and further in view of Applicant's Admitted Prior Art ("AAPA").

As per claim 2, Gupta teaches that the above selection device may be placed between the logic circuit and the power supply instead of ground (Col. 8, lines 5-10),

Gupta does not expressly teach having two separate switches – one providing a virtual ground and one for providing a virtual V_{dd}. AAPA teaches providing two such switches (Fig. 2). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply AAPA's virtual V_{dd} to Gupta's microprocessor. A motivation for doing so would have been to prevent loss of information to the logic circuit (Page 3, lines 11-15).

As per claim 5, Gupta teaches waiting a number of instruction cycles before processing the instruction (Col. 9, lines 40-45) and therefore teaches the register is updated after a number of instruction cycles.

As per claims 10 and 13, since Gupta/AAPA teaches the microprocessor of claims 2 and 5, the combination teaches the claimed microprocessor.

10. Claims 6, 8, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta as applied to claims 1 and 9 above, and further in view of Bertin et al., U.S. Patent No. 6,345,362 ("Bertin"). Bertin was cited in the previous office action.

As per claim 6, Gupta does not expressly teach determining anticipated usage using an input table including an instruction sequence and associated resource needs. Bertin teaches such an input table (Col. 5, lines 24-50). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Bertin's input table to Gupta's microprocessor.

As per claim 8, Bertin teaches an output table including logical states corresponding to power/saving on/off states of the at least one logical unit (Col. 5, lines 24-50).

As per claims 14 and 16, since Gupta/Bertin teaches the microprocessor of claims 6 and 8, the combination teaches the claimed microprocessor.

11. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bartley as applied to claim 17 above, and further in view of Gupta et al., U.S. Patent No. 5,996,083 ("Gupta"). Gupta was cited by the Applicant in the IDS filed November 21, 2003.

As per claim 21, Bartley does not expressly teach a number of cycles needed to execute an instruction sequence to turn each logical circuit on or off. Gupta teaches such a number (Col. 6, lines 14-28, value stored in latency control register). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Gupta's power latency value to Bartley's method. A motivation for doing so would have been to prevent error due to prematurely issuing an instruction (Col. 9, lines 40-45).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 703-305-5385. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

aw
June 11, 2004

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